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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,699	12/01/2003	Francois X. Prinz	24317/82501	2551
37803	7590	05/09/2008		EXAMINER
SIDLEY AUSTIN LLP 555 CALIFORNIA STREET SUITE 2000 SAN FRANCISCO, CA 94104-1715				BEHM, HARRY RAYMOND
			ART UNIT	PAPER NUMBER
			2838	
MAIL DATE	DELIVERY MODE			
05/09/2008	PAPER			

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/725,699	<b>Applicant(s)</b> PRINZ ET AL.
	<b>Examiner</b> HARRY BEHM	<b>Art Unit</b> 2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 14 March 2008.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 2,3,7,15 and 17-21 is/are pending in the application.
- 4a) Of the above claim(s) 15 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 2,3,7,17-21 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-166/08)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments concerning Corsi (US 5,912,551) or Duffy (US 2002/0171985), filed 3/14/08, have been fully considered but they are not persuasive.

Applicant argues the duty cycle generator, digital counter and first comparator of Corsi do not constitute an algorithm generator, but does not explain why the components do not constitute an algorithm generator. Oddly, Applicant does not dispute the duty cycle generator, digital counter and the first comparator produce an algorithm that determines the rate of change for modifying the duty cycle. Components that produce an algorithm by definition comprise an algorithm generator. Applicant has claimed an output of the algorithm is to adjust the rate of change for modifying the duty cycle, but has not claimed any of the steps in the algorithm. Since all controllers contain an algorithm generator to determine and adjust the duty cycle, Applicant has not differentiated the claimed invention from the prior art. All that is required of the claimed algorithm generator is to determine and adjust the rate of change for modifying the duty cycle. The algorithm generator of Corsi executes the steps necessary to determine and adjust the duty cycle, and therefore must determine and adjust the rate of change of the duty cycle.

Applicant further argues Corsi does not disclose adjusting the rate of change for modifying the duty cycle, but Corsi discloses adjusting the duty cycle which inherently involves adjusting the rate of change for modifying the duty cycle.

Applicant argues Duffy does not disclose changing the frequency of alteration of the duty cycle and states no duty cycle is depicted in Fig. 14. The on time of the duty cycle of each phase is depicted by the ramp rising, and the off time is depicted by the ramp falling. The duty cycle of each phase is typically altered once each switching period to regulate the output voltage, so the frequency of alteration of the duty cycle is typically performed at the switching frequency. When a large change in load occurs to a new reference (Fig. 14 1460), the frequency of alteration of the duty cycle is increased (Fig. 14 time 1450) from the switching frequency to quickly respond to the load. At time 1450, the frequency of alteration of the duty cycle is clearly increased to be faster than the switching frequency, thereby minimizing a dip in the output voltage.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Corsi (US 5,912,551).

A digital control system for controlling a switch (Fig. 1 10) of a voltage converter, comprising:

a duty cycle generator (Fig. 1 22 and Fig. 2 46,44) that provides a duty cycle [on/off time to gate of power switch] for the switch (Fig. 1 10);  
a digital counter [Fig. 1 20 is depicted as a counter, but only flip flops 40 and 42 in Fig. 2 create the counter] that stores a plurality of entries [two bit counter shown], wherein each entry (Fig. 2 Q1z,Q2) can be input [input to 46] to the duty cycle generator (Fig. 1-2 46,44,22) for modifying the duty cycle [gate signal on/off time] in response to a varying load [change in load causes Vout to deviate from Vref, which changes the count];  
a first comparator (Fig. 1 28) that compares an output voltage (Fig. 1 Vout) to a reference voltage (Fig. 1 Vref); and  
an algorithm generator (Fig. 1 20-32) producing an algorithm that determines the rate of change [duty cycle changed at rate in response to load] of for modifying the duty cycle;  
wherein if the first comparator (Fig. 1 28) detects that the output voltage is higher than the reference voltage, the algorithm generator [signal Vcom] affecting the input of entries from the digital counter [counter reset] into the duty cycle generator, thereby adjusting the rate of change for modifying the duty cycle of the switch [switching prevented].

Claims 7 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Duffy (US 2002/0171985).

With respect to Claim 7, Duffy discloses method for producing a desired output voltage (Fig. 12 Vo) comprising:

storing in memory (Fig. 8 730), an indication [error voltage used to generate duty cycle] of a duty cycle [on/off time of power switch] needed for a varying load (Fig. 6 530); monitoring the load (Fig. 6 VSENP,VSENN,ATRHC,ATRLC);

altering the duty cycle (on/off switching of power switches) at a first frequency (Fig. 14 initial frequency in which transient support (Fig. 6 540) is not used) to produce the desired output voltage (Fig. 6 572) based upon the indication; and

if a change in the load is detected (Fig. 9 910 comparator detect outside of window), changing the frequency (Fig. 14 at time 1450 some phases duty cycle changed early) of alteration of the duty cycle;

wherein if the load increases (Fig. 14 1450), the frequency of alteration is increased (Fig. 6 540 quickly activates switches by changing duty cycle early), thereby minimizing a dip in the output voltage [increased output current minimized output voltage drop].

With respect to Claim 17, Duffy discloses the method of claim 7 wherein monitoring the load (Fig. 6 530) comprises usage of two (Fig. 9 910) or more comparators.

With respect to Claim 18, Duffy discloses the method of claim 17 wherein the two (Fig. 6 602,604) or more comparators each have a different reference (Fig. 6 Vref+Δb1,Vref-Δb1).

With respect to Claims 19-21, Duffy discloses a voltage converter. See claims 7 and 17-18 for item matching.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Corsi (US 5,912,551) in view of Ogasawara (US 6,377,428).

With respect to Claim 3, Corsi discloses the system of claim 2. Corsi does not disclose a second comparator. Ogasawara teaches an overcurrent comparator (Fig. 1 CMP1) for controlling a switch of voltage converter. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a second comparator with a different voltage reference. The reason for doing so is for "detecting an abnormality" (Ogasawara column 1 line 10), such as an overcurrent, undervoltage, overvoltage or undervoltage.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HARRY BEHM whose telephone number is (571)272-8929. The examiner can normally be reached on 7:00 am - 3:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry Behm/  
Examiner, Art Unit 2838

/Jeffrey L. Sterrett/  
Primary Examiner, Art Unit 2838